# Proof of concept for through silicon vias in application-specific integrated circuits for hard x-ray imaging detectors

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**Abstract.** Application-specific integrated circuits (ASICs) are commonly used to efficiently process the signals from sensors and detectors in space. Wire bonding is a space-qualified technique of making interconnections between ASICs and their substrate packaging board for power, control, and readout of the ASICs. Wire bonding is nearly ubiquitous in modern space programs, but their exposed wires can be prone to damage during assembly and subject to electric interference during operations. Additional space around the ASICs needed for wire bonding also impedes efficient packaging of large arrays of detectors. Here, we introduce the through silicon vias (TSV) technology that replaces wire bonds and eliminates their shortcomings. We have successfully demonstrated the feasibility of implementing TSVs to existing ASIC wafers (a.k.a. a via-last process) developed for processing the x-ray signals from the x-ray imaging CdZnTe detectors on the Nuclear Spectroscopic Telescope Array small explorer telescope mission that was launched in 2012. While TSVs are common in the semiconductor industry, this is the first (to our knowledge) successful application for astrophysics imaging instrumentation. We expect that the TSV technology will simplify the detector assembly and thus will enable significant cost and schedule savings in assembly of large area CdZnTe detectors. *© 2021 Society of Photo-Optical Instrumentation Engineers (SPIE)* [DOI: 10.1117/1.JATIS.7.2.026001]

**Keywords:** application-specific integrated circuits; x-ray; CdZnTe detectors; wire bond; through silicon vias.

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## 1 Introduction and Motivation

The discovery and study of the most energetic transient astrophysics phenomena (in order of decreasing luminosity) include gamma-ray bursts of both long and short duration, outbursts from supermassive black holes (particularly blazars) in galactic nuclei, black hole and neutron star mergers discovered as gravitational wave outbursts, flaring outbursts from black hole and neutron star x-ray binaries, and extreme flares from single M-dwarf stars. These studies are best pursued by wide-field coded aperture hard x-ray telescopes. The high-resolution energetic x-ray imager (HREXI) is the high-resolution imaging 3- to 300-keV x-ray detector designed for optimum readout of a wide-field coded aperture telescope. Two wide-field, high-resolution mission concepts that employ the HREXI architecture are described by Grindlay et al.[1]

HREXI is composed of close-tiled high spatial resolution CdZnTe (CZT) detectors. The main heritage of CZT detectors in HREXI comes from the application-specific integrated circuit (ASIC) used in Nuclear Spectroscopic Telescope Array (NuSTAR)[2] and the large CZT detector plane (256 $\text{cm}^2$) assembled for a series of balloon-borne wide-field hard x-ray imaging telescope

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experiments ProtoEXIST1 & 2.[3–6] Each 0.3-cm-thick CZT crystal in HREXI has an active imaging area of $1.92 \times 1.92\ \mathrm{cm}^2$ with $32 \times 320.6$ mm pixels that are each conductive-epoxy bonded to the corresponding $32 \times 32$ pixels on a NuSTAR ASIC (hereafer NuASIC). HREXI groups CZT-NuASICs into a $2 \times 2$ close-tiled detector crystal array (DCA) that is read out and individually controlled as a single unit. But unlike NuSTAR, HREXI allows DCAs themselves to be close-tiled into arbitrarily large area detector arrays for large area coded aperture imaging with the wide field and sensitivity needed for the discovery and study of the energetic transients listed above. What is needed to make HREXI-based missions feasible is a technology to enable high-yield fabrication and assembly of a large area array of high-resolution CZT detectors for multiple wide-field telescopes at relatively low cost.

For ProtoEXIST1 & 2 and NuSTAR, the electrical connection between the NuASIC and the substrate board was made through wire bonding, where each of the 87 wire-bond pads on the NuASIC is connected to the matching pad on the substrate board underneath through a thin metal wire. Wire bonding is a space-qualified technique, commonly used for many electronics devices including detectors and sensors. However, the exposed wires are prone to damage during handling, and they can complicate the assembly procedure for a large detector array. They can be a source of electrical noise pickup during operation. Protecting wire bonds through potting or similar methods can also invite additional electronics noise. In addition, their presence introduces a significant gap between CZT detectors, making it difficult to closely tile the detectors into a large array. The NuASIC extends about 2.5 mm from the edge pixels on the wire-bond pad side, and the matching pads on the substrate board requires an additional 2.5-mm gap for safe wire bond installation and protection during assembly. Thus, with wire bonds, the gap between CZT crystals is about 5 mm on the wire-bond side. With through silicon vias (TSVs), this gap can shrink down to 2.5 mm for the current NuASICs, and the layout of new ASICs in future can be designed to further minimize this gap with TSVs (see Sec. 5). The large gaps between the detectors introduce additional background x-ray events and spatial nonuniformity in the background by allowing x-rays to enter the detectors through the side walls of CZT crystals (e.g., Fig. 7 in Ref. 5).

For the last few years, we have been pursuing the TSV technology to replace wire bonds and thus eliminate their shortcomings in CZT detector packaging. With TSVs, the power, control, and readout lines in an ASIC can be directly connected to the substrate board through the full Si layer in the ASIC, enabling flip-chip style bonding. Therefore, TSVs make the subsequent assembly procedures of detectors robust and simple, and it is projected that they would enable significant saving in cost and schedule for the assembly of a large array CZT detector plane. TSVs are implemented at a wafer level on multiple wafers in a single run, whereas wire bonding requires labor on the individual ASIC dies. CZT detectors can be tiled more tightly with TSVs by minimizing wasted space in between detectors. In this paper, we present the first successful implementation of TSVs in the current NuSTAR wafers.

An increasing number of vendors in the semiconductor industry now routinely utilize TSVs for "vertical" [three-dimensional (3-D)] packaging of ICs such as memory modules. The typical size of these TSVs is $\sim 5\ \mu\mathrm{m}$ in diameter and 15 to 50 $\mu$m in depth. They are often designed and fabricated in parallel with the IC circuitry under the careful layout of stacking geometry: i.e., they are implemented through a "via-middle" process, where TSVs are inserted during foundry runs for the ICs, typically after transistor fabrication but prior to back end of the line metalization.

While the via-middle procedure is the safest approach, redesigning existing ASICs for TSVs requires considerable resources, often prohibitively expensive under the relatively low funding of astrophysics instrumentation programs. Instead, we have decided to first demonstrate the feasibility and benefits of TSVs through a "via-last procedure," where the TSVs are inserted into the prefabricated ASICs on a wafer. The "via-last" approach can also be applied to other similar programs that can benefit from removal of wire bonds. One can further divide the via-last procedure into two different approaches: one inserting blind-TSVs from the back side of the wafer, and the other inserting through-TSVs from the front side. The successful TSV implementation demonstrated in this paper has utilized both approaches.

In this paper, we describe the methodology and performance of the back-side blind-TSV approach by vendor #1 in Secs. 2 and 3. In Sec. 4, we describe the concept and advantages of the front-side through-TSV insertion by vendor #2—Micross Advanced Interconnect

Technology (AIT),[7] and present the results of the performance measurements from the initial test run. Section 5 presents our vision of future detector assembly and packaging concept using the TSV technology.

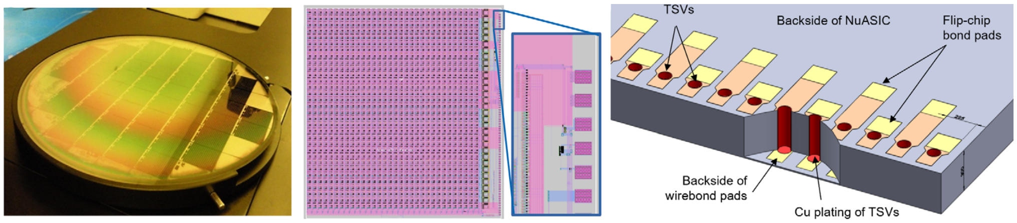
## 2 Implementing Back-Side Blind-TSVs on NuASIC Wafers

NuASICs are fabricated by ON Semiconductor Corp. on 700-$\mu$m-thick 8-in. silicon wafers. Each wafer has 49 NuASIC dies. Figure 1(a) shows a picture of a mechanical (dummy) version of the NuSTAR wafer, which was used for the process development of TSV insertion. Each NuASIC is equipped with 1024 gold stud pixels in a $32 \times 32$ two-dimensional array, matching the anode pattern of 1024 conductive epoxy dot pixels on a CZT crystal (0.6-mm pixel pitch), to which the NuASIC bonds directly.[5,8] The 87 wire-bond pads, with 225 $\mu$m pitch, that require electric connection are located along one edge of each NuASIC die [the right-hand side in Fig. 1(b)]. The silicon substrate underneath the wirebond pads is free of circuitry, making the NuSTAR wafers suitable for the via-last procedure.

Figure 1(c) shows a conceptual cutaway view of the back-side blind-TSVs that connect the flip-chip style bonding pads on the back side of the ASIC to the aluminum wire-bond pads on the front side. The basic idea for the back-side TSVs is to implement about 100 $\mu$m diameter by 300 $\mu$m deep TSVs from the back side of the wafer and touch down on the back of the wire-bond pads. The NuASIC has three metal layers and the wire-bond pads have all three layers electrically connected through internal vias to maximize the mechanical stability during the wire-bonding process. Thus, connecting the TSVs to the back of the metal 3 layer is equivalent to the electric connection to the wire-bond pad on the top metal layer.

Figure 2 shows the fabrication processes of back-side blind-TSVs by vendor #1. To achieve a high yield, the aspect ratio of the TSV height to diameter should be kept less than ~3 to 5. Since the wire-bond pads are about 150 $\mu$m $\times$ 120 $\mu$m, we settled on TSVs of 100 $\mu$m diameter. (A) To keep the aspect ratio low, we polish NuSTAR wafers down to 300 $\mu$m from the 700 $\mu$m thickness of the original NuASIC wafer. (B) The TSV profile is chemically etched out from the back side. (C) The etched TSVs are passivated with $SiO_2$ to insulate the surrounding Si in the substrate, and a Ta barrier layer is deposited to prevent Cu diffusion into the Si substrate. (D) Apply directionally sensitive reactive ion etch to reopen the passivation deposited on the back of the wire-bond pads. (E) The TSVs are metalized with Cu through multiple stages of sputtering. The back-side traces and flip-chip pads are plated in parallel. A final passivation is also applied to protect the TSVs and traces (not shown in the figure).

Initially, the vertical (cylinder shape) profile was adopted for TSVs, but it turns out that with the vertical profile, the Cu plating process results in excessive accumulation of Cu around the entrance of the TSVs, leaving little or no Cu plating near the back of the wire-bond pads. After exploring a few options to mitigate the issue, a tapered profile (funnel shape) for TSVs was adopted, which dramatically improved the uniformity in Cu metalization. Figure 3 compares the SEM images of the TSVs with vertical (left) and tapered (right) profiles. In the former, the Cu (light gray) tends to get accumulated around the opening of the TSVs while the Cu plating



(a) (b) (c)

**Fig. 1** (a) A mechanical wafer with 49 ASIC dies was used to develop the TSV process. (b) Each NuSTAR ASIC has 87 wire-bond pads on one edge for power, control, and readout. The inset shows a closeup view of six wire-bond pads with 225 $\mu$m pitch. (c) Cutaway view of back-side blind-TSV concept for NuSTAR ASIC (NuASIC). TSVs connect the flip-chip bonding pads on the back side of the ASIC to the back of the wire-bond pads on the front side of the NuASIC.

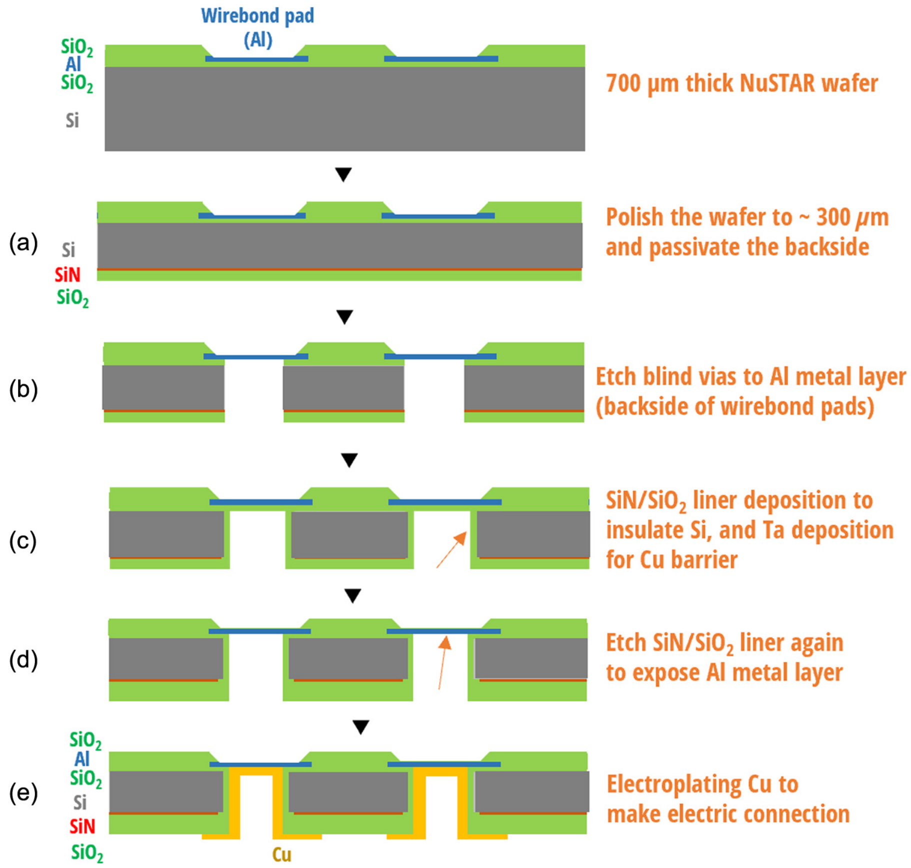
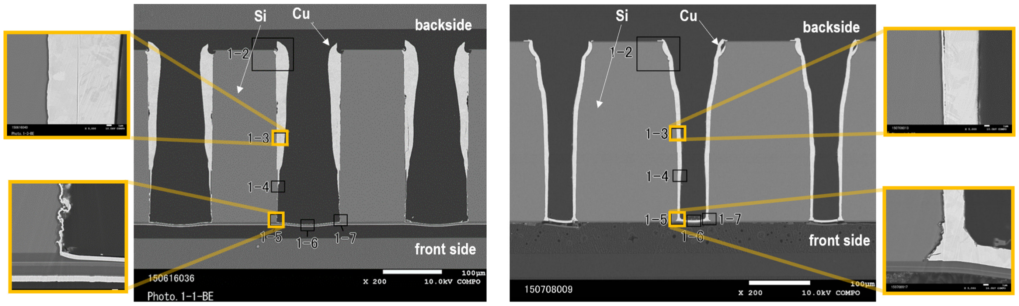

Wirebond pad
(Al)
$SiO_2$
Al
$SiO_2$
Si
700 μm thick NuSTAR wafer
(a)
Si
SiN
$SiO_2$
Polish the wafer to ~ 300 μm
and passivate the backside
(b)
Etch blind vias to Al metal layer
(backside of wirebond pads)
(c)
$SiN/SiO_2$ liner deposition to
insulate Si, and Ta deposition
for Cu barrier
(d)
Etch $SiN/SiO_2$ liner again
to expose Al metal layer
(e)
$SiO_2$
Al
$SiO_2$
Si
SiN
$SiO_2$
Cu
Electroplating Cu to
make electric connection

**Fig. 2** Back-side blind-TSV fabrication processes by vendor #1: (a) back-side polishing and passivation. (b) Blind TSV etching. (c) TSV passivation and Cu-barrier layer installation. (d) Exposing the bottom passivation of TSVs through directionally sensitive etching. (e) Electroplating Cu on TSVs to make electric connection.


Si
Cu
backside
1-2
1-3
1-4
1-5
1-6
1-7
front side
150616036
Photo. 1-1-BE
x 200
100μm
10.0kV COMPO
Si
Cu
backside
1-2
1-3
1-4
1-5
1-6
1-7
front side
150708009
x 200
100μm
10.0kV COMPO

(a) (b)

**Fig. 3** SEM images of back-side blind-TSV profiles by vendor #1: (a) vertical profile with cylinder shape. (b) Tapered profile with funnel shape.

lacks near the back of the wire-bond pads, resulting in poor conductivity. In contrast, the tapered TSV has the Cu layer uniformly plated along the entire profile of TSVs, providing good electrical connectivity.

## 3 Performance of NuSTAR ASIC with Back-Side Blind-TSVs

For diagnostic purpose, each NuASIC is equipped with internal pulser injection capability, which can trigger the readout sequence in the ASIC. The pulser charges deposited in a group of user-defined pixels by the internal pulser can be readout just like normal x-ray events. Since the pulser source is external, the overall spectral resolution of the pulser measurement is subject to stability of the external source, the build quality of the probe card used for testing ASIC dies, and the ASIC functionality. We have developed a probe card with a proper probe pin arrangement suitable for operation from the back side of ASICs through the TSVs. The card circuitry is identical to the one used for testing the original NuASIC wafers from the front side through the wire-bond pads.

Figure 4 compares a histogram of internal pulser signals measured through the front-side wire-bond pads (black) with the same through the back-side TSVs (red) from a NuASIC (die #47) with blind-TSVs of vertical profile. The histograms are the sum of the pulser readout from the triggered pixels, where the first 53 pixels were injected with pulser signals. The spectral resolution of the internal pulser signals is substantially degraded when measured through TSVs (5.4% FWHM) relative to the wire-bond pads (3% FWHM). In addition, both measurements, either through TSVs or wire-bond pads, show noticeable noise events near 0 ADU. Many pixels also exhibit noise signals above the threshold even without pulser injection: e.g., the measurements through the TSVs triggered 72 pixels even though only 53 pixels were injected with pulser signals.

This NuASIC is from the first attempt to implement TSVs from the back side, using the vertical profile. Typically NuASICs (without TSVs) have about 90% yield, but after the TSV insertion, only about 5 to 6 NuASICs out of 98 NuASICs show some response to external operational commands even when they are probed from the wire-bond pads. Die #47 is the only functioning (albeit temporary; see below) device out of 98 NuASICs from the two wafers that had undergone complete TSV insertion processes. In fact, all the partially functioning dies also exhibit a high current draw in the power line, which suggests that the TSV insertion in the first run introduced a kind of short or current leak somewhere in the system. Die #47 also stopped functioning after a few operations. We suspect that the current leak permanently damaged the ASIC.

As shown in the left panel in Fig. 3, inspection of the high-resolution SEM images of several TSV profiles revealed uneven etching surface of the TSV profiles especially near the bottom of the TSVs, suggesting potential electrical shorts between the Cu metal in the TSV and the Si substrate. We could not pinpoint any actual spot of electrical shorts from the SEM images, which is not surprising, given the limited cross-sections one can explore through a few SEM images.

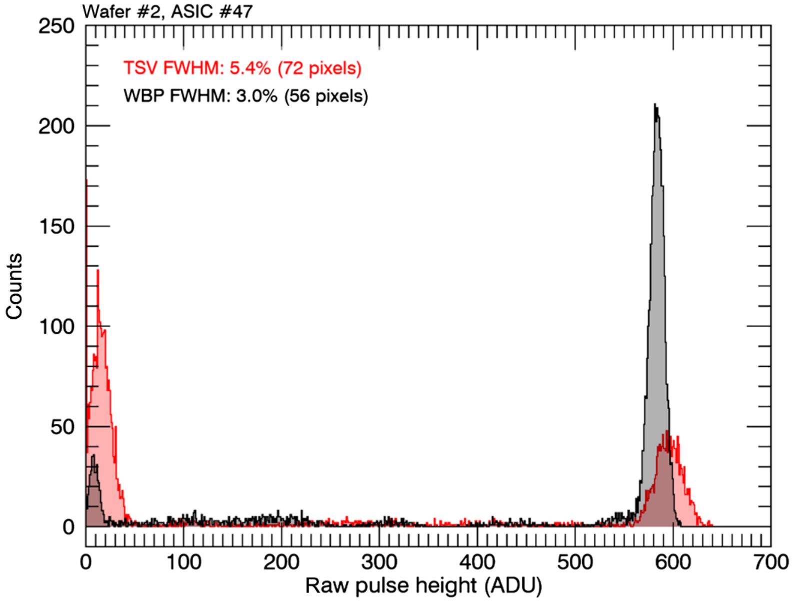


**Fig. 4** Pulser spectra comparison between wire-bond pads and blind-TSVs with vertical profiles from wafer #2 die #47 by vendor #1. The measurements through the TSVs degrade the spectral resolution, and both measurements show additional noise events near 0 ADU.

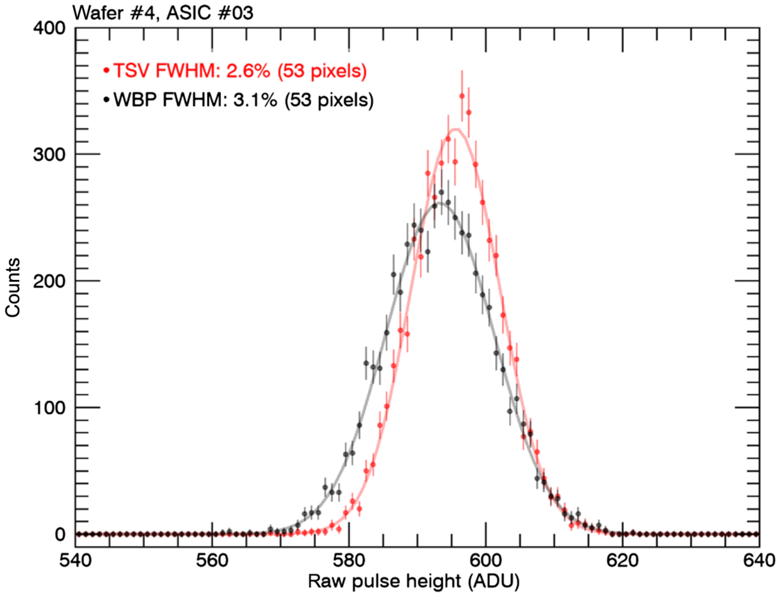


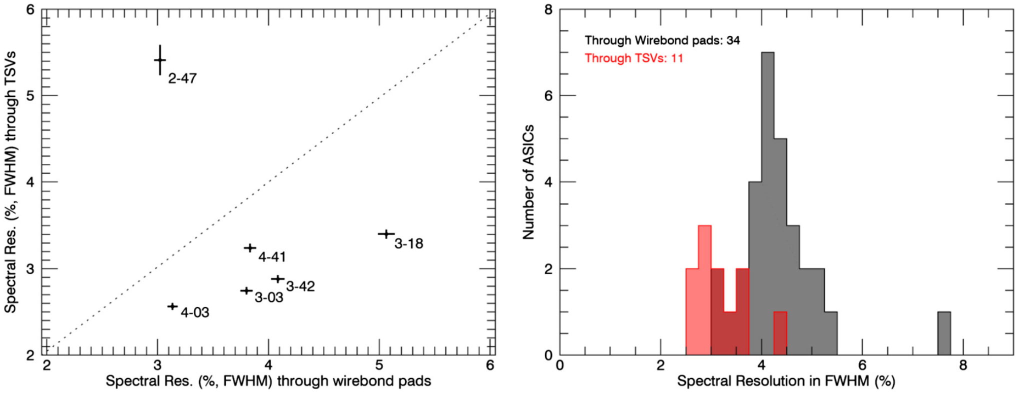
**Fig. 5** Pulser spectra comparison between wire-bond pads and blind-TSVs with tapered profiles from wafer #3 die #3 by vendor #1. The measurements through the TSVs show an improvement in the spectral resolution, compared to the measurements through the wire-bond pads.

Regardless, to mitigate the issue, the passivation layer of the TSVs were doubled for the second TSV run which utilized the tapered TSV profiles instead of the vertical profiles.

Figure 5 compares internal pulser measurements of a pixel on one of the NuASICs through wire-bond pads before TSV insertion and through TSVs after successful insertion of TSVs with tapered profiles. The spectrum measured through the TSVs shows an improvement in the spectral resolution (2.6% FWHM) relative to the measurements conducted through the wire-bond pads before TSV insertion (3.1% FWHM). These ASICs with tapered profile TSVs show no excessive noise events and their performance is stable over time, unlike die #47 in the earlier run. Despite the fact that the signal path length is slightly longer by as much as ∼1 mm when probed through the TSVs compared to the wire-bond pads, the improved spectral resolution in the measurements through TSVs is encouraging. In a completed detector assembly, the electrical paths through wire bonds are longer and more exposed than those through TSVs, and thus the system with TSVs is expected to be less susceptible to external noises. Note that pulser measurements of NuASICs depend on the stability of the external pulser source and the build quality of the probe cards as well as the ASIC performance. Nonetheless, the results indicate that the proper TSV insertion process does not degrade the ASIC performance.

Figure 6(a) compares the pulser measurements of the NuASICs where measurements through both wire-bond pads and TSVs are available for the same ASIC. Each data point is labeled by wafer and ASIC die IDs. Note the measurements through wire-bond pads for ASICs in wafers #3 and #4 were conducted before TSV insertion. TSVs in wafer #2 have vertical profiles, and ones in wafers #3 and #4 have tapered profiles. All the NuASICs with tapered profile TSVs show improvements in the pulser resolution when measured through TSVs compared to wire-bond pads. Figure 6(b) shows all the measurements we have conducted for ASICs in wafers #3 and #4, where the measurements through TSVs statistically outperform the measurements through wire-bond pads in spectral resolution, indicating a successful demonstration of the proof of concept for the via-last process for TSVs. The overall yield of the successful TSV implementation in wafers #3 and #4 is about 70% after accounting for the overall non-TSV NuASIC yield (90%).

Despite the relatively high yield in successful TSV implementation, we were not successful in assembling fully functioning CZT detectors from these TSV NuASICs. One of the main causes was excessive plating of back-side traces and bonding pads in part due to inexperience in trace plating of vendor #1. As a result, many traces were shorted to each other, making a large number of dies unusable. Overplating also introduced unnecessary stress in the wafers, which resulted in large cracks in the wafers during the debonding process of the carrier layer. The



(a) (b)

**Fig. 6** Spectral resolution comparison between wire-bond pads and blind-TSVs by vendor #1. (a) the ASIC dies with both measurements available. (b) Resolution distribution of all the measurements for wafers #3 and #4.

carrier layer is temporarily attached to protect thin wafers during the TSV implementation. The cracks further reduced the number of workable dies. Only 17 out of 98 NuASICs from the two wafers were properly plated for the traces and pads on the back side. In the case of wafer #4, the carrier layer debonding was abandoned due to the risk of cracking, which renders all the ASICs unusable for subsequent detector assembly since the carrier layer blocks access to the pixel pads on the front side.

Debonding of the carrier layer from wafer #3 revealed another weakness in the TSV implementation from the back side. Since TSVs touch down on the back of the wire-bond pads and the majority volume of the TSVs is not filled, the structural integrity of wire-bond pads is compromised after TSV insertion. As a result, the debonding process often delaminates parts or all of some wire-bond pads (Fig. 7), which makes the ASIC unusable either through TSVs or wire bonds. Only one (wafer #3 die #47) out of the 11 functioning TSV NuASICs survived the debonding process without loss of wire-bond pads and functions properly after the assembly with the substrate board.

Another weakness of the back-side TSV implementation is in the nature of the blind vias. It is difficult to reach and process the region where TSVs touch down on the wire-bond pads. The touch-down region also tends to develop unwanted chemical reactions and leave chemical

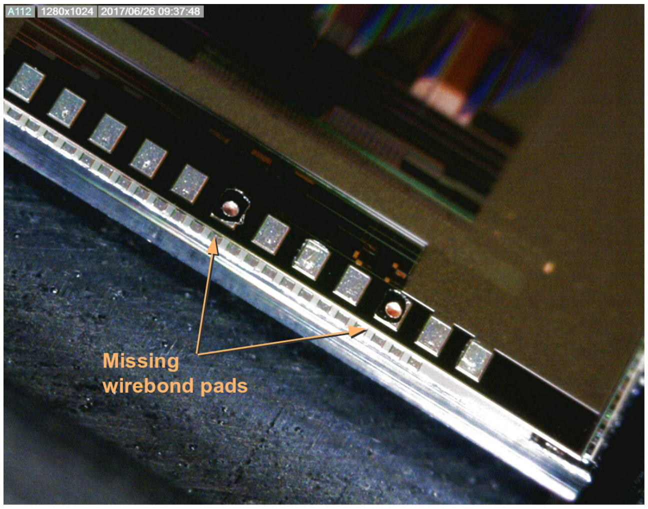


**Fig. 7** Loss of wire-bond pads during carrier layer debonding for blind-TSV implementation by vendor #1. Among 12 wire-bond pads visible in this view, two pads were delaminated during the debonding process of the carrier layer, which revealed the TSVs underneath.

residue while undergoing the multiple processes of etching and plating. This residue is often difficult to clean. As a result, this approach requires relatively expensive wafer processing tools, to which small vendors may not have access. In contrast, relatively large wafer processing vendors do have these necessary tools, but they often do not show interest in small volume development projects like ours. Unfortunately, vendor #1, which performed the runs described in the above sections, stopped offering TSV services needed for our development after a recent corporate restructuring, and we had to search for other vendors. We did regroup with a new vendor that retained some of the key members from vendor #1 who had worked on our TSV development effort. The subsequent attempt with the new vendor to implement back-side blind-TSVs, however, was unsuccessful due to lack of necessary tools, despite a few novel ideas to address the challenges.

## 4 Front-Side Through-TSVs and Their Performance

With the successful proof of the TSV concept, we searched for a new approach that enables high yield in detector assembly with relatively easily accessible tools. A promising approach is the implementation of true through-silicon vias from the front side of wafers (instead of back-side blind-TSVs). This approach resolves the difficulties in the previous runs with TSV etching, metallization, and interconnection to the ASIC bond pads. We have finished the initial test run of implementing front-side TSVs on 3 NuASIC wafers with our current industry partner, AIT.

Figure 8 shows the fabrication processes of the front-side through-TSVs. (A) The front side of the wafer is passivated and the (vertical) profiles of TSVs are etched out next to wire-bond pads. (B) After properly passivating the TSVs with $SiO_2$ and depositing the Cu-barrier layers (TiN) to prevent Cu diffusion into the Si wafer, the TSVs are Cu-filled along with the front surface. (C) The front-side Cu deposit is polished off so that the wafer surface is planarized with $SiO_2$ remaining over the Al pad, and then, both wire-bond pads and pixel pads are exposed through etching. (D) The Ni/Au traces connecting TSVs to wire-bond pads are deposited on the front side, and then the back side is polished and etched to expose the TSVs. (E) Passivate the back side and deposit the proper metal traces and solder bump pads on the back side for flip-chip bond.

This approach does not disturb the Si substrate below the wire-bond pads on the front side of the original NuASIC, so there is no risk of weakening or losing any wire-bond pads in the process. The Cu metal is deposited inside the TSVs after the TSVs profiles are etched blind (C), but the blind end of the TSVs is revealed again through dry etch after polishing, so there is no concern of developing any complex chemical residues that require careful cleaning and monitoring. This in turn enables use of relatively small vias (20 $\mu$m diameter). These small TSVs are fully Cu-filled, improving the mechanical integrity of each die.

Our relatively small TSVs allow three TSV insertions for each wire-bond pad, improving the yield in conductivity. Figure 9 shows a small region around a few wire-bond pads during TSV implementation: (A) the front side after Cu-filling TSVs (three TSVs per wire-bond pad), (B) the front side after Ni/Au trace layout connecting TSVs to an edge of each wire-bond pad, (C) the bottom side showing the TSVs, flip-chip style pads, and connecting traces, and (D) an SEM image of the TSV cross section. As mentioned, we inserted three TSVs for each wire-bond pad in between each wire-bond pad. We laid out the connecting traces between TSVs and the wire-bond pads. The majority of the original Al wire-bond pads are exposed so that in principle wire bonding can be applied to these ASICs if needed. The pads for flip-chip style bonding on the back side are now made in a circular shape [instead of the original rectangular shape; see Fig. 1(c)] in order to improve the uniformity in the spherical solder ball attachment and spread, which in turn improves bonding quality. The pads are coated with Ni and Au to avoid oxidization.

Figure 10 shows the pulser performance measured through the TSVs (red) in comparison with the same through the wire-bond pads (black). The measurements through the wire-bond pads were done before the TSV implementation. Some of the measurements through the TSVs were done using the ASIC test setup (ATS) developed at Harvard.[9,10] The ATS is designed to

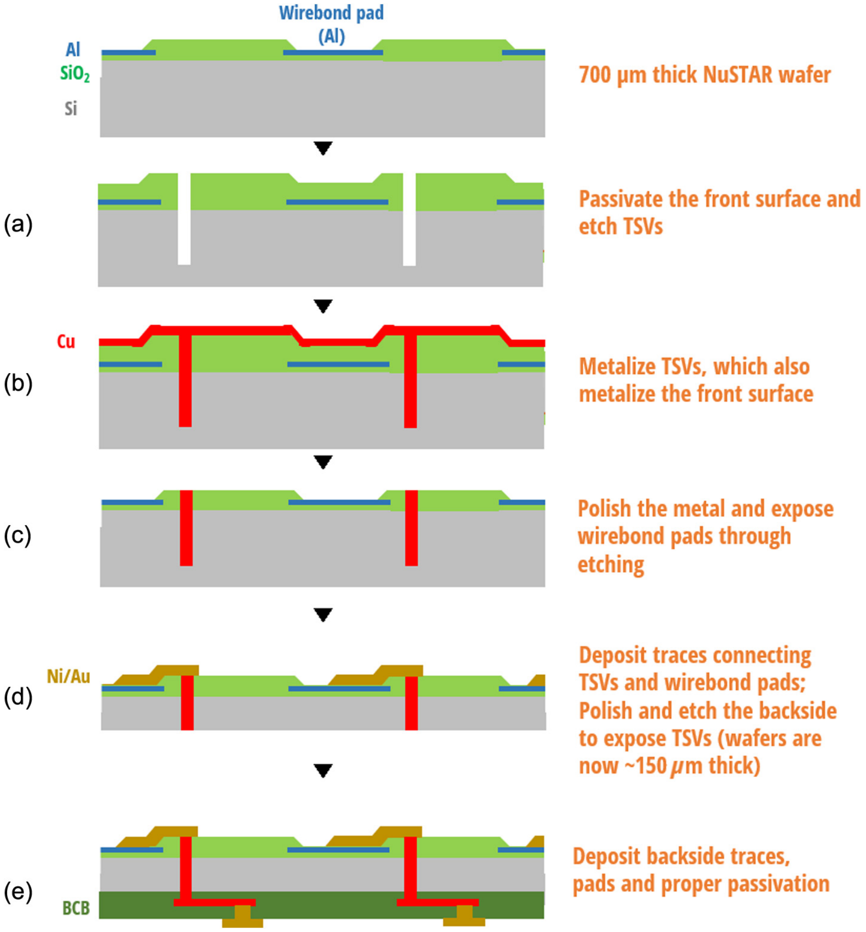

Wirebond pad
(Al)
Al
SiO2
Si
700 µm thick NuSTAR wafer
(a)
Passivate the front surface and etch TSVs
Cu
(b)
Metalize TSVs, which also metalize the front surface
(c)
Polish the metal and expose wirebond pads through etching
Ni/Au
(d)
Deposit traces connecting TSVs and wirebond pads; Polish and etch the backside to expose TSVs (wafers are now ~150 µm thick)
(e)
BCB
Deposit backside traces, pads and proper passivation

**Fig. 8** Front-side through-TSV fabrication processes by vendor #2 (Micross AIT): (a) front-side passivation and TSV etching. (b) TSV and front-side metalization. (c) Exposing wire-bond pads through chemical-mechanical polishing, surface planarizing, and etching. (d) Deposition of traces connecting TSVs and wire-bond pads, and exposing TSVs from the back side through polishing followed by etching. (e) Trace and pad deposition on the back side along with proper passivation.

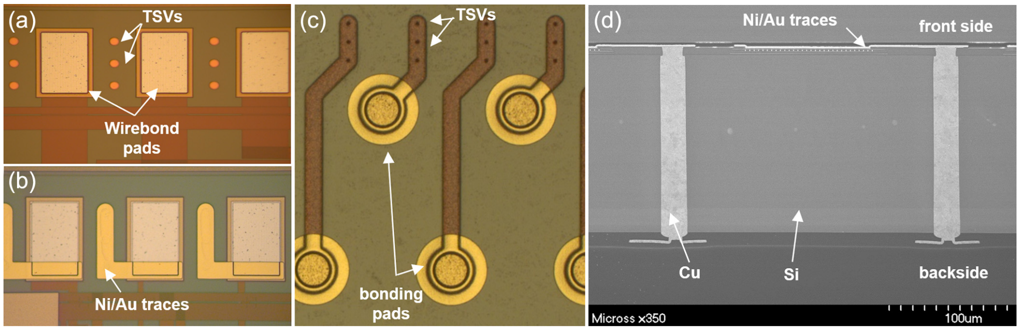

(a)
TSVs
Wirebond
pads
(b)
Ni/Au traces
(c)
TSVs
bonding
pads
(d)
Ni/Au traces
front side
Cu
Si
backside
Micross x350
100um

**Fig. 9** Progress of the through-TSV implementation by vendor #2 (Micross AIT): (a) the front side after TSV Cu-filling and polishing, showing TSVs next to wire-bond pads (three TSVs per wire-bond pad were employed), (b) the front side with traces connecting TSVs to wire-bond pads, (c) the back side showing TSVs, solder bump pads and connecting traces, and (d) an SEM image of the TSVs.

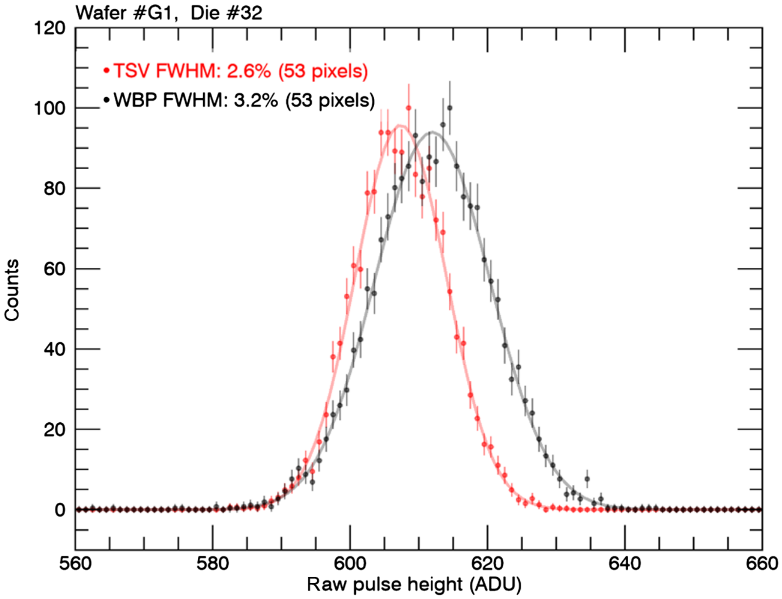


**Fig. 10** Pulser performance of a NuASIC with front-side TSVs by vendor #2 (Micross AIT): measurements through TSVs (red) in comparison with the same through wire-bond pads (black).

enable rapid test and screening of TSV ASICs through quick and easy alignment of pogo-pins and the back-side pads or solder bumps on the pads of the ASIC. The distribution is a sum of the pulser data from the first 53 pixels of wafer #G1 and die #32. This demonstrates the successful operations in the ASICs with front-side through-TSVs. The overall spectral resolution improved again with the TSVs relative to the operation through wire-bond pads.

Among 15 font-side TSV NuASICs that were tested so far, four NuASICs show a good pulser performance (similar to Fig. 10) in the initial pulser runs, showing about 30% of yield. While this yield appears to be small relative to the earlier run, we believe that the yield is nearly 100% in terms of the conductivity of TSVs. In this initial run for the front-side TSVs, a set of daisy chained TSVs are inserted to each ASIC die for diagnostic purpose, where the electrical conductivity and isolation of TSVs can be tested.[7] According to the conductivity test of the daisy chain, the average resistivity of TSVs is less than 1Ω with practically 100% yield. The cause of the relatively low yield in the overall functionality is suspected to be the insufficient isolation or insulation of the TSVs.

In fact, all of the tested ASICs draw the increasingly higher current in the power line over time during the pulser tests and eventually became unresponsive after about 10 min of operation. Subsequent power cycle would start the ASIC at a relatively higher current draw state even after a few days of nonoperation, and the ASICs become unresponsive within a minute. This result is consistent with the isolation tests of the daisy chain TSVs, where the current leak between relatively nearby TSVs (electrically unconnected) was observed to increase over time.[7]

While we are investigating the root cause of this current instability, the observed symptoms resemble what we had experienced with the very first run of the back-side blind-TSV implementation, where all the dies draw high currents in the power line and their functionality was unstable. The most likely cause is the insufficient thickness for the $SiO_2$ insulation and/or Cu barrier layer surrounding each TSV as well as between the Cu traces and underlying Si wafer. In fact, the first run of the back-side blind-TSV implementation had issues in both TSV conductivity and isolation, which resulted in a poor spectral resolution (Fig. 4) and a low yield (∼1%). It is clear that the front-side through-TSVs in this first trial run have good conductivity but poor insulation according to both the pulser and daisy chain tests. We plan to increase the thickness of $SiO_2$ insulation and Cu barrier layers, which had resolved the similar issue for the back-side blind-TSVs. As we learn more about the cause of the high current draw and instability, we will further revise the processes, which will be applied in the next run for the front-side through-TSV implementation. Given the good conductivity of the front-side TSVs, we expect that the overall

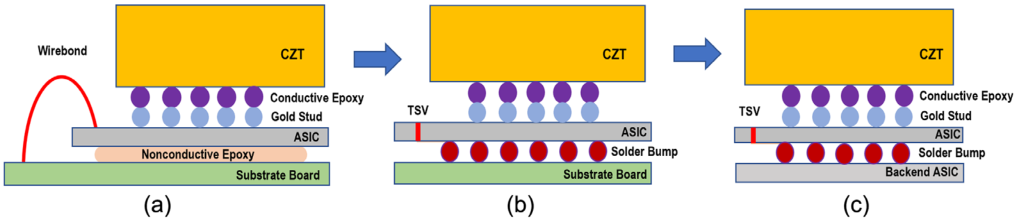


**Fig. 11** (a) CZT and ASIC assembly using wire bonds. (b) The same with TSVs. (c) CZT, ASIC and backend ASIC assembly using 3-D stacking.

yield for successful NuASICs with front-side TSVs will exceed the 70% yield in the back-side TSV NuASICs of the second-run once we resolve the TSV isolation issue.

## 5 Summary and Detector Assembly with TSVs

We presented the first successful proof of concept for TSVs to replace wire bonds for readout and control of ASICs bonded to CZT imaging detectors. We used two approaches. While both are viable, the approach using front-side through-TSVs resolves major weaknesses in the other approach using back-side blind-TSVs, enabling an easier and cleaner path for both TSV insertion and final detector assembly.

With the TSV NuASICs, we can envision true 3-D stacking of the backend electronics for CZT detector assembly in future as shown in Fig. 11. The current design of our CZT detector assembly employs a set of field programmable gate arrays (FPGAs) and complex programmable logic devices to control and readout the NuASICs. These logic devices are mounted in the substrate board where the NuASICs are mounted and connected through wire bonds [Fig. 11(a)]. With TSVs, assembly between the CZT crystal, the NuASIC, and the substrate board is achieved essentially through a series of flip-chip style bonding [Fig. 11(b)]. Once the operational code of the logic devices is well defined and frozen, the front end of the FPGAs can be turned into another signal-processing ASIC, which can be directly 3-D stacked underneath the ASIC using TSVs [Fig. 11(c)]. The design of NuASIC itself can be further optimized to minimize the gap between the CZT crystals. One can go a step further, the layout of both the NuASIC and the signal processing ASIC can be designed with TSVs in mind. The TSV technology enables easy, robust, and low-cost assembly and packaging concept to a wide range of detector and sensor systems.

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